

# SANYO Semiconductors **DATA SHEET**

## LC875J96B LC875J80B LC875J72B

CMOS IC
ROM 96K/80K/72K byte, RAM 4096 byte on-chip
8-bit 1-chip Microcontroller

#### Overview

The SANYO LC875J96B/80B/72B are 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 96K/80K/72K byte ROM, 4096 byte RAM, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a 16-bit timer with a prescaler (may be divided into 8-bit timers), a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO interface, a UART interface (full duplex), an 8-bit 11-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, ROM correction function, and a 26-source 10-vector interrupt feature.

#### **Features**

#### **■**ROM

98304 × 8-bits (LC875J96B)
 81920 × 8-bits (LC875J80B)
 73728 × 8-bits (LC875J72B)

#### **■**RAM

•  $4096 \times 9$ -bits (LC875J96B/80B/72B)

### ■Minimum Bus Cycle

83.3ns (12MHz) V<sub>DD</sub>=3.0 to 5.5V
 125ns (8MHz) V<sub>DD</sub>=2.5 to 5.5V
 500ns (2MHz) V<sub>DD</sub>=2.2 to 5.5V

Note: The bus cycle time here refers to the ROM read speed.

- Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.
- Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

### **SANYO Semiconductor Co., Ltd.**

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

#### ■Minimum Instruction Cycle Time

250ns (12MHz) V<sub>DD</sub>=3.0 to 5.5V
 375ns (8MHz) V<sub>DD</sub>=2.5 to 5.5V
 1.5μs (2MHz) V<sub>DD</sub>=2.2 to 5.5V

#### ■Ports

• Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1-bit units
46 (P1n, P2n, P70 to P73, P80 to P86, PBn, PCn, PWM2, PWM3, XT2)

Ports whose I/O direction can be designated in 4-bit units

• Normal withstand voltage input port

• Dedicated oscillator ports

• Deadt pins

Reset pinsPower pins

1 (RES) 6 (VSS1 to 3, VDD1 to 3)

8 (P0n)

1 (XT1)

2 (CF1, CF2)

### **■**Timers

• Timer 0: 16-bit timer/counter with two capture registers.

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)

Mode 3: 16-bit counter (with two 16-bit capture registers)

• Timer 1: 16-bit timer/counter that supports PWM/toggle outputs

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)

Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels

Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8-bits)

Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8-bits can be used as PWM)

- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 8: 16-bit timer

Mode 0: 8-bit timer with an 8-bit prescaler × 2 channels

Mode 1: 16-bit timer with an 8-bit prescaler

- \* Timer 8 is not supported in this version of Emulator. Please use on-chip-debugger (only supported in flash-ROM version) for debugging when developing software.
- Base Timer
  - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  - 2) Interrupts programmable in 5 different time schemes

### ■High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
- 2) Can generate output real-time.

#### **■**SIO

- SIO0: 8-bit synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  - 3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface

Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)

Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)

Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)

Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

#### **■**UART

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator
- ■AD Converter: 8-bits × 11 channels
- ■PWM: Multifrequency 12-bit PWM × 2 channels
- ■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
  - Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
- ■Watchdog Timer
  - External RC watchdog timer
  - Interrupt and reset signals selectable
- **■**Clock Output Function
  - 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
  - 2) Able to output oscillation clock of sub clock.

#### **■**Interrupts

- 26 sources, 10 vector addresses
  - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/T8L/T8H
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- IFLG (list of interrupt source flag function)
  - 3) Shows a list of interrupt source flags that caused a branching to a particular vector address (shown in the diagram above).
- ■Subroutine Stack Levels: 2048 levels (the stack is allocated in RAM)
- ■High-speed Multiplication/Division Instructions
  - 16-bits × 8-bits (5 tCYC execution time)
     24-bits × 16-bits (12 tCYC execution time)
  - 16-bits ÷ 8-bits (8 tCYC execution time)
  - 24-bits ÷ 16-bits (12 tCYC execution time)

#### ■Oscillation Circuits

• RC oscillation circuit (internal): For system clock

• CF oscillation circuit: For system clock, with internal Rf

• Crystal oscillation circuit: For low-speed system clock, with internal Rf

• Frequency variable RC oscillation circuit (internal): For system clock

#### ■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

#### ■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) Canceled by a system reset or occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The CF, RC, and crystal oscillators automatically stop operation.
  - 2) There are three ways of resetting the HOLD mode.
    - (1) Setting the reset pin to the low level.
    - (2) Setting at least one of the INTO, INT1, INT2, INT4, and INT5 pins to the specified level
    - (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  - 1) The CF and RC oscillators automatically stop operation.
  - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  - 3) There are four ways of resetting the X'tal HOLD mode.
    - (1) Setting the reset pin to the low level
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    - (3) Having an interrupt source established at port 0
    - (4) Having an interrupt source established in the base timer circuit

#### **■**ROM Correction Function

- Executes the correction program on detection of a match with the program counter value.
- Correction program area size: 128 bytes

#### ■Package Form

QIP64E (14 × 14): Lead-free type
TQFP64J (10 × 10): Lead-free type

#### **■**Development Tools

• Evaluation chip: LC87EV690

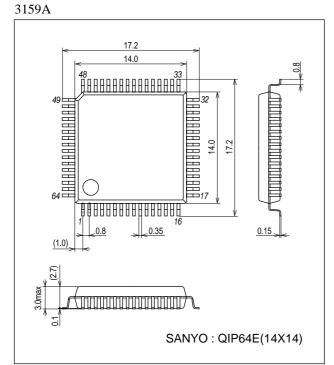
• Emulator: EVA62S + ECB876600D + SUB875800 + POD64QFP or POD64SQFP

 $ICE-B877300 + SUB875800 + POD64QFP \ or \ POD64SQFP$ 

• On-chip debugger: TCB87-TypeA or TCB87-TypeB + LC87F5JC8A

### **Package Dimensions**

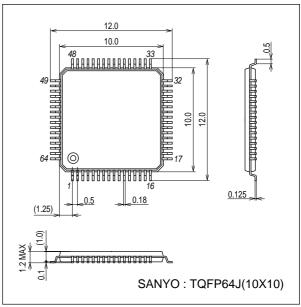
unit: mm (typ)



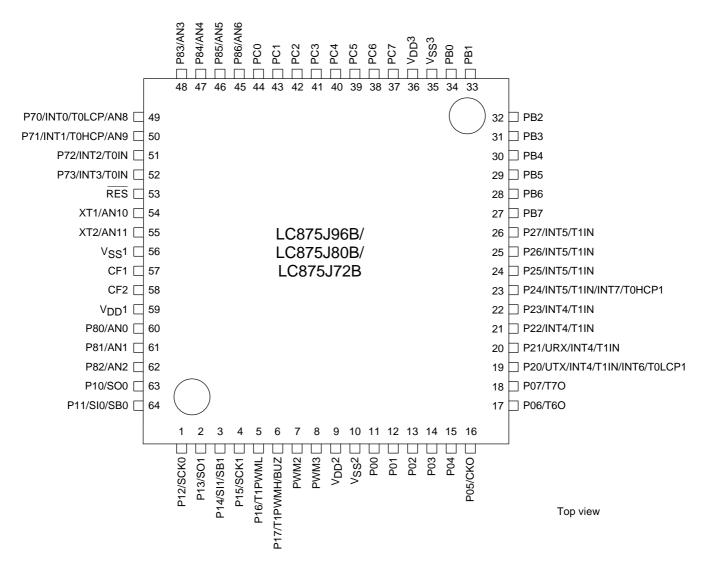
### **Package Dimensions**

unit : mm (typ)

3310

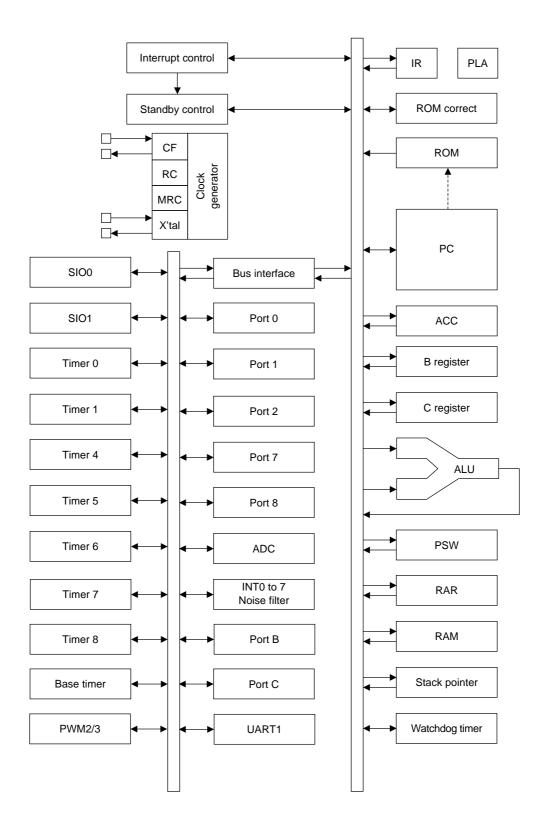


### **Pin Assignment**



SANYO: QIP64E(14×14) "Lead-free Type" SANYO: TQFP64J(10×10) "Lead-free Type"

### **System Block Diagram**



### **Pin Description**

Pin Name	I/O			De	scription			Option
V <sub>SS</sub> 1	-	- Power supply	pin					No
$V_{SS}^2$								
V <sub>SS</sub> 3								
V <sub>DD</sub> 1	-	+ Power supply	pin					No
$V_{DD}^2$								
$V_{DD}3$								
Port 0	I/O	• 8-bit I/O port						Yes
P00 to P07		I/O specifiable	in 4-bit units					
		Pull-up resistor	rs can be turned	d on and off in 4-	bit units.			
		HOLD reset in	put					
		Port 0 interrup	t input					
		<ul> <li>Shared pins</li> </ul>						
		P05: Clock ou	tput (system clo	ck/can selected	from sub clock)			
		P06: Timer 6 t	oggle output					
		P07: Timer 7 t	oggle output					
Port 1	I/O	8-bit I/O port						Yes
P10 to P17		I/O specifiable						
			rs can be turned	d on and off in 1-	bit units.			
		Pin functions						
		P10: SIO0 dat	-					
			a input/bus I/O					
		P12: SIO0 clo						
		P13: SIO1 dat	•					
			a input/bus I/O					
		P15: SIO1 clo						
		P16: Timer 1P						
			WMH output/be	eper output				
Port 2	I/O	8-bit I/O port						Yes
P20 to P27		I/O specifiable		1 1 . 661 . 4	1.9			
		· ·	rs can be turned	d on and off in 1-	bit units.			
		Pin functions	:4					
		P20: UART tra						
		P21: UART re		roact input/time	. 1 avant innut/tin	nor OL conturo in	nut/	
			•	•	i eveni inputiti	ner 0L capture in	pui/	
			mer 0H capture	-	. 1 ovent input/tir	ner 0L capture in	nut/	
			mer 0H capture	•	i event inputui	nei or capture in	puv	
			ut/timer 0L capt	•				
		•	ut/timer 0E capt ut/timer 0H capt					
		Interrupt acknow		aro i input				
		Thorrapt dollro	<u> </u>		Rising &			
			Rising	Falling	Falling	H level	L level	
		INT4	enable	enable	enable	disable	disable	
		INT5	enable	enable	enable	disable	disable	
		INT6	enable	enable	enable	disable	disable	
		INT7	enable	enable	enable	disable	disable	
			00010	00010	00010	G.04010	0.00010	

Continued on next page.

Continued from preceding page.

Pin Name	I/O				Option				
Port 7	I/O	• 4-bit I/O port						No	
P70 to P73		I/O specifiable	e in 1-bit units						
		Pull-up resiste	ors can be turne	d on and off in 1-l	oit units.				
		<ul> <li>Shared pins</li> </ul>							
		P70: INT0 inp	out/HOLD reset in	nput/timer 0L cap	ture input/watchd	og timer output			
		P71: INT1 inp	out/HOLD reset in	nput/timer 0H cap	ture input				
		P72: INT2 inp	2: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/						
		High sp	High speed clock counter input						
		P73: INT3 inp	: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input						
		AD converter	AD converter input port: AN8 (P70), AN9 (P71)						
		Interrupt ackno	wledge type			T	T		
			Rising	Falling	Rising & Falling	H level	L level		
		INT0	enable	enable	disable	enable	enable		
		INT1	enable	enable	disable	enable	enable		
		INT2	enable	enable	enable	disable	disable		
		INT3	enable	enable	enable	disable	disable		
Port 8	I/O • 7-bit I/O port							No	
P80 to P86		I/O specifiable	e in 1-bit units						
		Shared pins							
		AD converter	input port: AN0	(P80) to AN6 (P8	6)				
PWM2, PWM3	I/O	PWM2 and P	WM3 output port	s				No	
		General-purp	ose I/O available	1					
Port B	I/O	• 8-bit I/O port						Yes	
PB0 to PB7		I/O specifiable	e in 1-bit units						
		Pull-up resiste	ors can be turne	d on and off in 1-l	oit units.				
Port C	I/O	8-bit I/O port						Yes	
PC0 to PC7		I/O specifiable	e in 1-bit units						
		Pull-up resiste	ors can be turne	d on and off in 1-l	oit units.				
RES	Input	Reset pin						No	
XT1	Input	• 32.768kHz cr	ystal oscillator in	put pin				No	
		<ul> <li>Shared pins</li> </ul>							
		General-purp	ose input port						
		AD converter	input port: AN10	)					
		Must be conne	cted to V <sub>DD</sub> 1 if r	not to be used.					
XT2	I/O	• 32.768kHz cr	ystal oscillator o	utput pin				No	
		Shared pins							
		General-purp	ose I/O port						
		AD converter	input port: AN1	I					
		Must be set for	oscillation and k	ept open if not to	be used.				
CF1	Input	Ceramic reson	ator input pin					No	
CF2	Output	Ceramic reson	ator output pin					No	

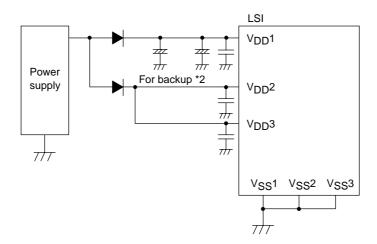
### **Port Output Types**

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1-bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P86	-	No	Nch-open drain	No
PWM2, PWM3	-	No	CMOS	No
PB0 to PB7	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PC0 to PC7	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
XT1	-	No	Input for 32.768kHz crystal oscillator (Input only)	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

\*1: Connect the IC as shown below to minimize the noise input to the  $V_{DD}1$  pin. Be sure to electrically short the  $V_{SS}1$ ,  $V_{SS}2$ , and  $V_{SS}3$  pins.



\*2: The internal memory is sustained by V<sub>DD</sub>1. If none of V<sub>DD</sub>2 and V<sub>DD</sub>3 are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time.

Make sure that the port outputs are held at the low level in the HOLD backup mode.

### **Absolute Maximum Ratings** at $Ta = 25^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		I		ication	1
				V <sub>DD</sub> [V]	min	typ	max	uni
Maximum supply voltage	V <sub>DD</sub> max	V <sub>DD</sub> 1, V <sub>DD</sub> 2, V <sub>DD</sub> 3	V <sub>DD</sub> 1=V <sub>DD</sub> 2=V <sub>DD</sub> 3		-0.3		+6.5	
Input voltage	V <sub>I</sub> (1)	XT1, CF1			-0.3		V <sub>DD</sub> +0.3	
Input/output voltage	VIO(1)	Ports 0, 1, 2						V
		Ports 7, 8			-0.3		V <sub>DD</sub> +0.3	
		Ports B, C PWM2, PWM3, XT2						
Peak output	IOPH(1)	Ports 0, 1, 2	CMOS output select		40			
current		Ports B, C	Per 1 applicable pin		-10			
	IOPH(2)	PWM2, PWM3	Per 1 applicable pin		-20			
	IOPH(3)	P71 to P73	Per 1 applicable pin		-5			
Mean output	IOMH(1)	Ports 0, 1, 2	CMOS output select		-7.5			
current	101411(0)	Ports B, C	Per 1 applicable pin					
(Note1-1)	IOMH(2)	PWM2, PWM3	Per 1 applicable pin		-15			
thdt	IOMH(3)	P71 to P73	Per 1 applicable pin		-3			
Total output	ΣΙΟΑΗ(1)	P71 to P73	Total of all applicable pins		-10			<u> </u>
Total output  Current  (Note1-1)  Total output  current	ΣΙΟΑΗ(2)	Port 1 PWM2, PWM3	Total of all applicable pins		-25			
Ĭ	ΣΙΟΑΗ(3)	Ports 0, 2	Total of all applicable pins		-25			
	ΣΙΟΑΗ(4)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins		-45			
	ΣΙΟΑΗ(5)	Port B	Total of all applicable pins		-25			
	ΣΙΟΑΗ(6)	Port C	Total of all applicable pins		-25			
	ΣΙΟΑΗ(7)	Ports B, C	Total of all applicable pins		-45			
Peak output	IOPL(1)	P02 to P07	Per 1 applicable pin					
current		Ports 1, 2					20	
		Ports B, C					20	
	IOPL(2)	PWM2, PWM3 P00, P01	Per 1 applicable pin				00	
	IOPL(3)	Ports 7, 8	Per 1 applicable pin				30	m
	IOPL(3)	XT2	Fei i applicable pili				10	
Mean output	IOML(1)	P02 to P07	Per 1 applicable pin					
current		Ports 1, 2					15	
(Note1-1)		Ports B, C					13	
ent	10141 (0)	PWM2, PWM3	D. A Facility 1					
cur	IOML(2)	P00, P01	Per 1 applicable pin				20	
ndtho	IOML(3)	Ports 7, 8 XT2	Per 1 applicable pin				7.5	<b>.</b>
Total output current current	ΣIOAL(1)	Port 7 P83 to P86, XT2	Total of all applicable pins				15	
Low	ΣIOAL(2)	P80 to P82	Total of all applicable pins				15	
	ΣIOAL(3)	Ports 7, 8 XT2	Total of all applicable pins				20	
	ΣIOAL(4)	Port 1 PWM2, PWM3	Total of all applicable pins				45	
	ΣIOAL(5)	Ports 0, 2	Total of all applicable pins				45	
	ΣIOAL(6)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins				80	}
	ΣIOAL(7)	Port B	Total of all applicable pins				45	ł
	ΣIOAL(8)	Port C	Total of all applicable pins				45	
	ΣΙΟΑL(9)	Ports B, C	Total of all applicable pins				80	
Power dissipation	Pd max	QIP64E (14 × 14)	Ta=-30 to +70°C				355	
		TQFP64J (10 × 10)					255	m'
Operating ambient	Topr				-30		+70	
temperature								•

Note 1-1: The mean output current is a mean value measured over 100ms.

### Allowable Operating Conditions at Ta = -30 °C to +70 °C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

					55	Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Operating	V <sub>DD</sub> (1)	V <sub>DD</sub> 1=V <sub>DD</sub> 2=V <sub>DD</sub> 3	0.245μs≤tCYC≤200μs	5511	3.0		5.5	
supply voltage			0.367μs≤tCYC≤200μs		2.5		5.5	
			1.470µs≤tCYC≤200µs		2.2		5.5	
Memory sustaining supply voltage	VHD	V <sub>DD</sub> 1=V <sub>DD</sub> 2=V <sub>DD</sub> 3	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	V <sub>IH</sub> (1)	Ports 1, 2 P71 to P73 P70 port input/ interrupt side		2.2 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	
	V <sub>IH</sub> (2)	Ports 0, 8, B, C PWM2, PWM3		2.2 to 5.5	0.3V <sub>DD</sub> +0.7		$V_{DD}$	
	V <sub>IH</sub> (3)	Port 70 watchdog timer side		2.2 to 5.5	0.9V <sub>DD</sub>		$V_{DD}$	V
	V <sub>IH</sub> (4)	XT1, XT2, CF1 RES		2.2 to 5.5	0.75V <sub>DD</sub>		$V_{DD}$	
Low level input voltage	V <sub>IL</sub> (1)	Ports 1, 2 P71 to P73		4.0 to 5.5	V <sub>SS</sub>		0.1V <sub>DD</sub> +0.4	
		P70 port input/ interrupt side		2.2 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (2)	Ports 0, 8, B, C PWM2, PWM3		4.0 to 5.5	V <sub>SS</sub>		0.15V <sub>DD</sub> +0.4	
				2.2 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	
	V <sub>IL</sub> (3)	Port 70 watchdog timer side		2.2 to 5.5	V <sub>SS</sub>		0.8V <sub>DD</sub> -1.0	
	V <sub>IL</sub> (4)	XT1, XT2, CF1 RES		2.2 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
Instruction cycle	tCYC			3.0 to 5.5	0.245		200	
time				2.5 to 5.5	0.367		200	μs
(Note 2-1)				2.2 to 5.5	1.470		200	
External system clock frequency	FEXCF(1)	CF1	CF2 pin open     System clock frequency	3.0 to 5.5	0.1		12	
			division ratio=1/1 • External system clock duty	2.5 to 5.5	0.1		8	
			=50 ± 5%	2.2 to 5.5	0.1		2	
			CF2 pin open     System clock fraguency	3.0 to 5.5	0.2		24.4	
			System clock frequency division ratio=1/2	2.5 to 5.5	0.2		16	
				2.2 to 5.5	0.2		4	MHz
Oscillation frequency range	FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	3.0 to 5.5		12		IVITZ
(Note 2-2)	FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		8		
	FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		4		
	FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0	
	FmMRC		Frequency variable RC oscillation	2.2 to 5.5		16		
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.2 to 5.5		32.768		kHz

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-2: See Tables 1 and 2 for the oscillation constants.

### **Electrical Characteristics** at $Ta = -30^{\circ}C$ to $+70^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Doromotor	Cumbal	Pin/Remarks	Conditions			Specifi	cation	
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
High level input current	I <sub>IH</sub> (1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C RES PWM2, PWM3	Output disabled Pull-up resistor off VIN=VDD (Including output Tr's off leakage current)	2.2 to 5.5			1	
	I <sub>IH</sub> (2)	XT1, XT2	For input port specification  VIN=VDD	2.2 to 5.5			1	
	I <sub>IH</sub> (3)	CF1	V <sub>IN</sub> =V <sub>DD</sub>	2.2 to 5.5			15	
Low level input current	I <sub>IL</sub> (1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C RES PWM2, PWM3	Output disabled Pull-up resistor off  VIN=VSS (Including output Tr's off leakage current)	2.2 to 5.5	-1			μΑ
	I <sub>IL</sub> (2)	XT1, XT2	For input port specification VIN=VSS	2.2 to 5.5	-1			
	I <sub>IL</sub> (3)	CF1	V <sub>IN</sub> =V <sub>SS</sub>	2.2 to 5.5	-15			
High level output	V <sub>OH</sub> (1)	Ports 0, 1, 2	I <sub>OH</sub> =-1mA	4.5 to 5.5	V <sub>DD</sub> -1			
voltage	V <sub>OH</sub> (2)	Ports B, C	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (3)		I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (4)	P71 to P73	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (5)		I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (6)	PWM2, PWM3	I <sub>OH</sub> =-10mA	4.5 to 5.5	V <sub>DD</sub> -1.5			
	V <sub>OH</sub> (7)		I <sub>OH</sub> =-1.6mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (8)		I <sub>OH</sub> =-1mA	2.2 to 5.5	V <sub>DD</sub> -0.4			,,
Low level output	V <sub>OL</sub> (1)	Ports 0, 1, 2	I <sub>OL</sub> =10mA	4.5 to 5.5			1.5	V
voltage	V <sub>OL</sub> (2)	Ports B, C	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (3)	PWM2, PWM3	I <sub>OL</sub> =1mA	2.2 to 5.5			0.4	
	V <sub>OL</sub> (4)	Ports 7, 8	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (5)	XT2	I <sub>OL</sub> =1mA	2.2 to 5.5			0.4	
	V <sub>OL</sub> (6)	P00, P01	I <sub>OL</sub> =30mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (7)	1	I <sub>OL</sub> =5mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (8)	]	I <sub>OL</sub> =2.5mA	2.2 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 7	V <sub>OH</sub> =0.9V <sub>DD</sub>	4.5 to 5.5	15	35	80	1.0
	Rpu(2)	Ports B, C		2.2 to 5.5	18	50	150	kΩ
Hysteresis voltage	VHYS	RES Ports 1, 2, 7		2.2 to 5.5		0.1 V <sub>DD</sub>		٧
Pin capacitance	СР	All pins	For pins other than that under test:  VIN=VSS f=1MHz Ta=25°C	2.2 to 5.5		10		pF

# Serial Input/Output Characteristics at $Ta=-30^{\circ}C$ to $+70^{\circ}C$ , $V_{SS}1=V_{SS}2=V_{SS}3=0V$ 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

		Parameter	Symbol	Pin/Remarks	Conditions			Speci	fication	
	Г	arameter	Symbol	FIII/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
		Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.		2			
	×	Low level pulse width	tSCKL(1)				1			
	Input clock	High level pulse width	tSCKH(1)			2.2 to 5.5	1			10)(0
Serial clock	ul		tSCKHA(1)		Continuous data transmission/reception mode     See Fig. 6.     (Note 4-1-2)		4			tCYC
Serial		Frequency	tSCK(2)	SCK0(P12)	CMOS output selected     See Fig. 6.		4/3			
	ock	Low level pulse width	tSCKL(2)					1/2		tSCK
	Output clock	High level pulse width		2.2 to 5.5	1/2		took			
	Outpr		tSCKHA(2)		Continuous data transmission/reception mode CMOS output selected See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
input	Da	ta setup time	tsDI(1)	SB0(P11), SI0(P11)	Must be specified with respect to rising edge of SIOCLK.     See Fig. 6.		0.03			
Serial input	Da	ta hold time	thDI(1)			2.2 to 5.5	0.03			
	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	Continuous data transmission/reception mode     (Note 4-1-3)				(1/3)tCYC +0.05	μs
Serial output	Input		tdD0(2)		Synchronous 8-bit mode     (Note 4-1-3)	2.2 to 5.5			1tCYC +0.05	
Serie	Output clock		tdD0(3)		(Note 4-1-3)				(1/3)tCYC +0.05	

- Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.
- Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.
- Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

### 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

		Parameter	Cumbal	Pin/Remarks	Conditions			Speci	fication	
	1	Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
	×	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.		2			
	Input clock	Low level pulse width	tSCKL(3)			2.2 to 5.5	1			.0.(0
Serial clock	<u>l</u>	High level pulse width	tSCKH(3)				1			tCYC
Serial	ž	Frequency	tSCK(4)	SCK1(P15)	CMOS output selected     See Fig. 6.		2			
	Output clock	Low level pulse width	tSCKL(4)			2.2 to 5.5		1/2		tSCK
	ŏ	High level pulse width	tSCKH(4)					1/2		ISCK
Serial input	Da	ta setup time	tsDI(2)	SB1(P14), SI1(P14)	Must be specified with respect to rising edge of SIOCLK.     See Fig. 6.	001.55	0.03			
Serial	Da	ta hold time	thDI(2)			2.2 to 5.5	0.03			
Serial output	Οι	tput delay time	tdD0(4)	SO1(P13), SB1(P14)	Must be specified with respect to falling edge of SIOCLK.     Must be specified as the time to the beginning of output state change in open drain output mode.     See Fig. 6.	2.2 to 5.5			(1/3)tCYC +0.05	μs

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

### Pulse Input Conditions at Ta = -30 °C to +70 °C, $V_SS1 = V_SS2 = V_SS3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions			Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27), INT6(P20),	Interrupt source flag can be set.     Event inputs for timer 0 or 1 are enabled.	2.2 to 5.5	1			
	tPIH(2) tPIL(2)	INT7(P24) INT3(P73) when noise filter time constant is 1/1	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.2 to 5.5	2			tCYC
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.2 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	Interrupt source flag can be set.     Event inputs for timer 0 are enabled.	2.2 to 5.5	256			
	tPIL(5)	RES	Resetting is enabled.	2.2 to 5.5	200			μs

### **AD Converter Characteristics** at $Ta = -30^{\circ}C$ to $+70^{\circ}C$ , VSS1 = VSS2 = VSS3 = 0V

D	O: : h l	Dia /Danasalas	O a malistic man			Specifi	cation	
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Resolution	N	AN0(P80) to		3.0 to 5.5		8		bit
Absolute accuracy	ET	AN6(P86), AN8(P70),	(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD	AN9(P71), AN10(XT1), AN11(XT2)	AD conversion time=32xtCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	15.68 (tCYC= 0.49μs)		97.92 (tCYC= 3.06μs)	
			3.0 to 5.5	23.52 (tCYC= 0.735μs)		97.92 (tCYC= 3.06μs)		
			AD conversion time=64xtCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	18.82 (tCYC= 0.294μs)		97.92 (tCYC= 1.53μs)	μѕ
				3.0 to 5.5	47.04 (tCYC= 0.735μs)		97.92 (tCYC= 1.53μs)	
Analog input voltage range	VAIN			3.0 to 5.5	V <sub>SS</sub>		V <sub>DD</sub>	٧
Analog port	IAINH	1	VAIN=V <sub>DD</sub>	3.0 to 5.5			1	
input current	IAINL	1	VAIN=V <sub>SS</sub>	3.0 to 5.5	-1			μΑ

Note 6-1: The quantization error ( $\pm 1/2$ LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

 $\textbf{Consumption Current Characteristics} \ \, at \ \, Ta = -30^{\circ}C \ \, to \ \, +70^{\circ}C, \ \, V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$ 

Parameter	Symbol	Pin/	Conditions			Specif	fication	1							
	_ ,	Remarks	22300	V <sub>DD</sub> [V]	min	typ	max	unit							
Normal mode consumption current (Note 7-1)	IDDOP(1)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3	FmCF=12MHz     ceramic oscillation mode     FmX'tal=32.768kHz crystal     oscillation mode     System clock set to 12MHz side	4.5 to 5.5		8.5	14								
	IDDOP(2)		Internal RC oscillation stopped     Frequency variable RC oscillation stopped     1/1 frequency division ratio	3.0 to 3.6		4.8	8.5								
	IDDOP(3)		CF1=24MHz external clock     FmX'tal=32.768kHz crystal     oscillation mode     System clock set to CF1 side	4.5 to 5.5		10	16.5								
	IDDOP(4)		Internal RC oscillation stopped     Frequency variable RC     oscillation stopped     1/2 frequency division ratio	3.0 to 3.6		5.5	9.3								
	IDDOP(5)		FmCF=8MHz     ceramic oscillation mode     FmX'tal=32.768kHz crystal	4.5 to 5.5		5.8	9.4								
	IDDOP(6)		oscillation mode  • System clock set to 8MHz side  • Internal RC oscillation stopped	3.0 to 3.6		3.3	5.9								
	IDDOP(7)		Frequency variable RC oscillation stopped     1/1 frequency division ratio	2.5 to 3.0		2.4	4.2	mA							
	IDDOP(8)		<ul> <li>FmCF=4MHz         ceramic oscillation mode</li> <li>FmX'tal=32.768kHz crystal</li> </ul>	4.5 to 5.5		2.1	3.3								
	IDDOP(9)	- -	oscillation mode  • System clock set to 4MHz side  • Internal RC oscillation stopped	3.0 to 3.6		1.1	2.1								
	IDDOP(10)		Frequency variable RC oscillation stopped     1/2 frequency division ratio	2.2 to 3.0		0.8	1.5								
	IDDOP(11)		FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz crystal oscillation mode System clock set to internal RC oscillation Frequency variable RC oscillation	4.5 to 5.5		0.6	2.1								
	IDDOP(12)			3.0 to 3.6		0.35	1.4								
	IDDOP(13)		• 1/2 frequency division ratio	2.2 to 3.0		0.25	1								
	IDDOP(14)	FmCF=0Hz (oscillation stopped) FmX'tal=32.768kHz crystal oscillation mode Internal RC oscillation stopped System clock set to 1MHz with	4.5 to 5.5	o 5.5 1.25		3.6									
	IDDOP(15)										System clock set to 1MHz with	3.0 to 3.6		0.7	2.3
	IDDOP(17)	_	frequency variable RC oscillation  • 1/2 frequency division ratio  • FmCF=0Hz (oscillation stopped)	2.2 to 3.0		0.45	1.7								
	. ,	• Fr • Fr • os • Sy • In	FmX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		28	66								
	IDDOP(18)		System clock set to 32.768kHz side	3.0 to 3.6		12	46	μΑ							
	IDDOP(19)		stopped  • 1/2 frequency division ratio	2.2 to 3.0		8	32								

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pin/	Conditions			Specification			
		Remarks		V <sub>DD</sub> [V]	min	typ	max	unit	
HALT mode consumption current	IDDHALT(1)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3	HALT mode     FmCF=12MHz ceramic oscillation mode     FmX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		2.8	5.6		
(Note 7-1)	IDDHALT(2)		System clock set to 12MHz side     Internal RC oscillation stopped     Frequency variable RC oscillation stopped     1/1 frequency division ratio	3.0 to 3.6		1.5	3.1		
	IDDHALT(3)		HALT mode     CF1=24MHz external clock     FmX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		3.7	7.5		
	IDDHALT(4)		System clock set to CF1 side     Internal RC oscillation stopped     Frequency variable RC oscillation stopped     1/2 frequency division ratio	3.0 to 3.6		2	4.1		
	IDDHALT(5)		HALT mode     FmCF=8MHz ceramic oscillation mode	4.5 to 5.5		2.05	4.2		
	IDDHALT(6)		FmX'tal=32.768kHz crystal oscillation mode     System clock set to 8MHz side     Internal RC oscillation stopped	3.0 to 3.6		1.15	2.3		
	IDDHALT(7)		Frequency variable RC oscillation stopped     1/1 frequency division ratio	2.5 to 3.0		0.75	1.5	mA	
	IDDHALT(8)		HALT mode     FmCF=4MHz ceramic oscillation mode	4.5 to 5.5		1	2.1		
	IDDHALT(9)		FmX'tal=32.768kHz crystal oscillation mode     System clock set to 4MHz side     Internal RC oscillation stopped	3.0 to 3.6		0.5	1.1		
	IDDHALT(10)		Frequency variable RC oscillation stopped     1/2 frequency division ratio	2.2 to 3.0		0.3	0.7		
	IDDHALT(11)		HALT mode     FmCF=0Hz (oscillation stopped)	4.5 to 5.5		0.28 1 0.15 0.7			
	IDDHALT(12)		FmX'tal=32.768kHz crystal oscillation mode     System clock set to internal RC oscillation	3.0 to 3.6			0.7	-	
	IDDHALT(13)		Frequency variable RC oscillation stopped     1/2 frequency division ratio	2.2 to 3.0		0.1	0.5		
	IDDHALT(14)		HALT mode     FmCF=0Hz (oscillation stopped)     FmX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		1.05	2.9		
	IDDHALT(15)		Internal RC oscillation stopped     System clock set to 1MHz with	3.0 to 3.6		0.6	1.8		
	IDDHALT(16)		frequency variable RC oscillation  • 1/2 frequency division ratio	2.2 to 3.0		0.4	1.4		
	IDDHALT(17)		HALT mode     FmCF=0Hz (oscillation stopped)	4.5 to 5.5		19.2	51		
	IDDHALT(18)		FmX'tal=32.768kHz crystal oscillation mode     System clock set to 32.768kHz side     Internal RC oscillation stopped	3.0 to 3.6	6.3	30			
	IDDHALT(19)		Frequency variable RC oscillation stopped     1/2 frequency division ratio	2.2 to 3.0		3.7	20		
HOLD mode	IDDHOLD(1)	V <sub>DD</sub> 1	HOLD mode	4.5 to 5.5		0.015	10	μΑ	
consumption	IDDHOLD(2)		CF1=V <sub>DD</sub> or open (external clock mode)	3.0 to 3.6		0.009	7		
current	IDDHOLD(3)	]		2.2 to 3.0		0.006	6		
Timer HOLD	IDDHOLD(4)		Timer HOLD mode	4.5 to 5.5		16.2	46		
mode	IDDHOLD(5)	1	• CF1=V <sub>DD</sub> or open (external clock mode)	3.0 to 3.6		5.6	25		
consumption	IDDHOLD(6)	†	FmX'tal=32.768kHz crystal oscillation mode	2.2 to 3.0					

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

### **UART (Full Duplex) Operating Conditions** at $Ta = -30^{\circ}C$ to $+70^{\circ}C$ , $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

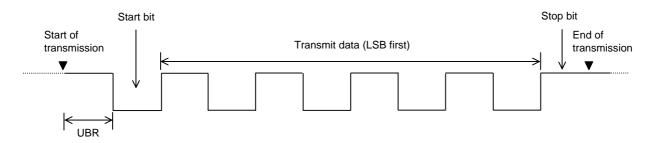
Danamatan	Cumahad	Pin/Remarks	Conditions		Specification				
Parameter	Symbol		Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Transfer rate	UBR	UTX(P20), URX(P21)		2.2 to 5.5	16/3		8192/3	tCYC	

Data length: 7, 8, and 9 bits (LSB first)

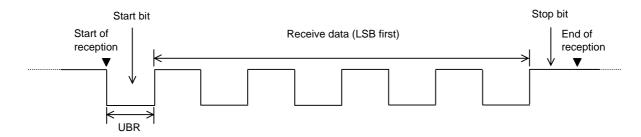
Stop bits: 1-bit (2-bit in continuous data transmission)

Parity bits: None

\*Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



\*Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)



### Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1	Characteristics	of a Sam	nle Main S	vstem Clock	Oscillator	Circuit with a	Ceramic Oscillator
I dolo I	Characteristics	or a barr	pic muni o	y btom Clock	Obcillator	Circuit With t	. Ceramic Obernator

Nominal Vendor Frequency Name	Vendor			Circuit	Constant		Operating Voltage	Oscil Stabilizat			
	Oscillator Name	C1 [pF]	C2 [pF]	Rf [Ω]	Rd1 [Ω]	Range [V]	typ [ms]	max [ms]	Remarks		
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	Open	470	3.0 to 5.5	0.1	0.5	Internal C1, C2	
8MHz MURATA	CSTCE8M00G52-R0	(10)	(10)	Open	2.2k	2.7 to 5.5	0.1	0.5	Internal		
		MURATA	CSTLS8M00G53-R0	(15)	(15)	Open	680	2.5 to 5.5	0.1	0.5	C1, C2
4MHz	MURATA	MURATA	CSTCR4M00G53-R0	(15)	(15)	Open	3.3k	2.2 to 5.5	0.2	0.6	Internal
			MURATA	CSTLS4M00G53-B0	(15)	(15)	Open	3.3k	2.2 to 5.5	0.2	0.6

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after  $V_{DD}$  goes above the operating voltage lower limit (see Figure 4).

### **Characteristics of a Sample Subsystem Clock Oscillator Circuit**

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name Oscil	On silled an News	Circuit Constant				Operating Voltage	Oscillation Stabilization Time		Damada
		Oscillator Name	C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]	Range [V]	typ [s]	max [s]	Remarks
32.768kHz	SEIKO EPSON	MC-306	18	18	Open	560k	2.2 to 5.5	1.4	3.0	Applicable CL value = 12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

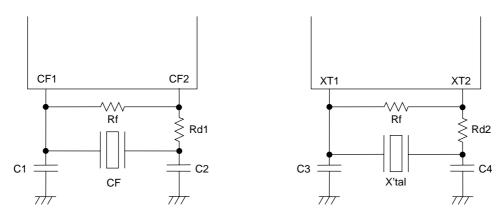
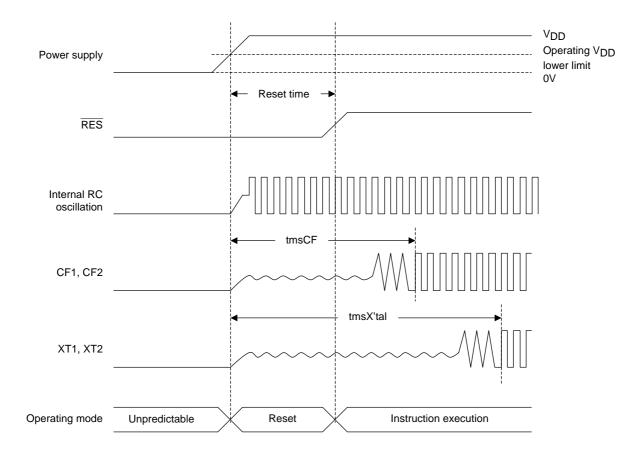


Figure 1 CF Oscillator Circuit

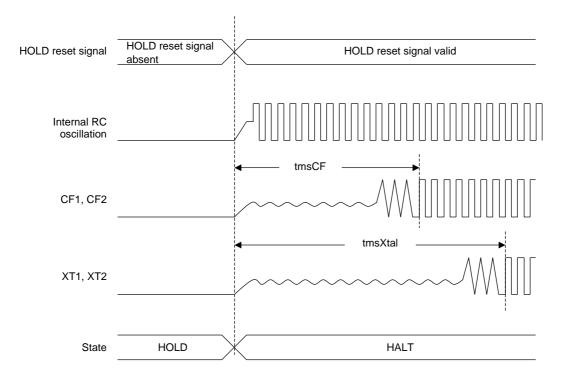
Figure 2 XT Oscillator Circuit



Figure 3 AC Timing Measurement Point

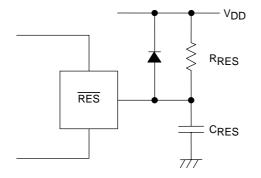


Reset Time and Oscillation Stabilizing Time



**HOLD Reset Signal and Oscillation Stabilization Time** 

Figure 4 Oscillation Stabilization Times



#### Note:

Determine the value of CRES and RRES so that the reset signal is present for a period of  $200\mu s$  after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

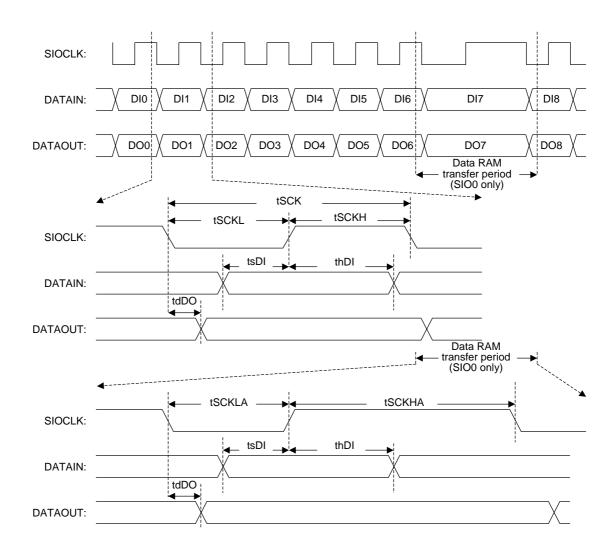


Figure 6 Serial I/O Output Waveforms

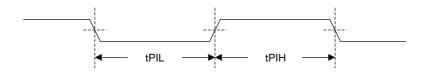


Figure 7 Pulse Input Timing Signal Waveform

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co..Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of February, 2007. Specifications and information herein are subject to change without notice.